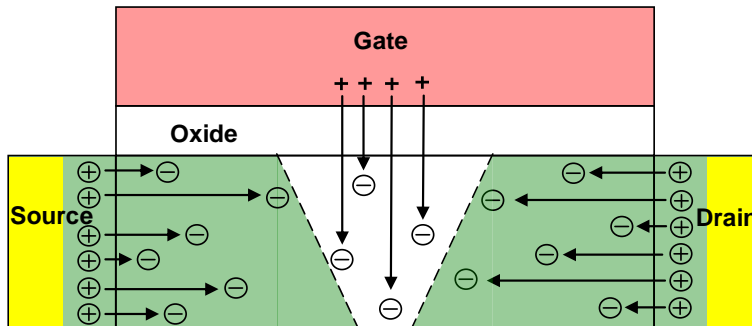
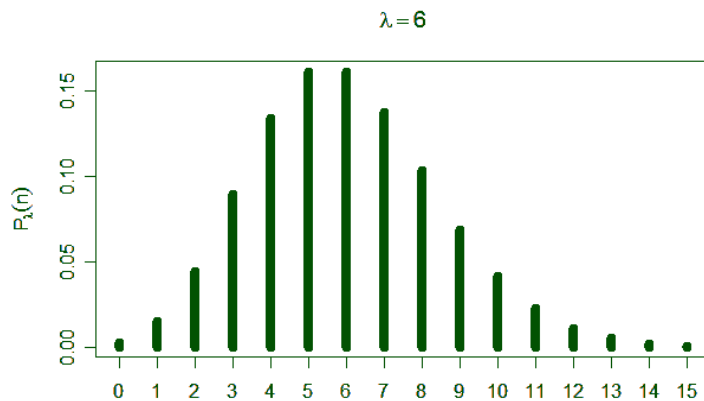


## Limits on the Nano-Roadmap

- **The Future of Eight Chip Technologies (chapter3)** by Bernd Hoefflinger



In this 10nm fully-depleted SOI NMOS Transistor, just 4 Boron atoms determine its threshold voltage. For a mean of 6 Boron atoms, 95% of all transistors would be controlled by 2 to 9 atoms, as shown below, a large fundamental variance setting a scaling limit.



- **ITRS-The International Technology Roadmap for Semiconductors (chapter 7)** by Bernd Hoefflinger
- **Nanolithography (chapter 8)** by Burn Lin, Vice President Lithography, TSMC, Hsinchu, Taiwan.

kW	Immer. scanner	EUV HVM			MEB HVM	
	Supplier estimate	Supplier estimate	30 mJ/cm <sup>2</sup> instead of 10 mJ/cm <sup>2</sup>	30 mJ/cm <sup>2</sup> resist + conservative collector and source efficiencies	Ten 10-wph columns	Share datapath
Source	89	580	1,740	16,313	120	120
Exposure unit	130	169	190	190		
Datapath					250	53
Total per tool	219	749	1,930	16,503	370	173
Total for 59 tools	12,921	44,191	113,870	973,648	21,830	10,222
Fraction of scanner power in fab	8.61%	29.46%	75.91%	649.10%	14.55%	6.81%

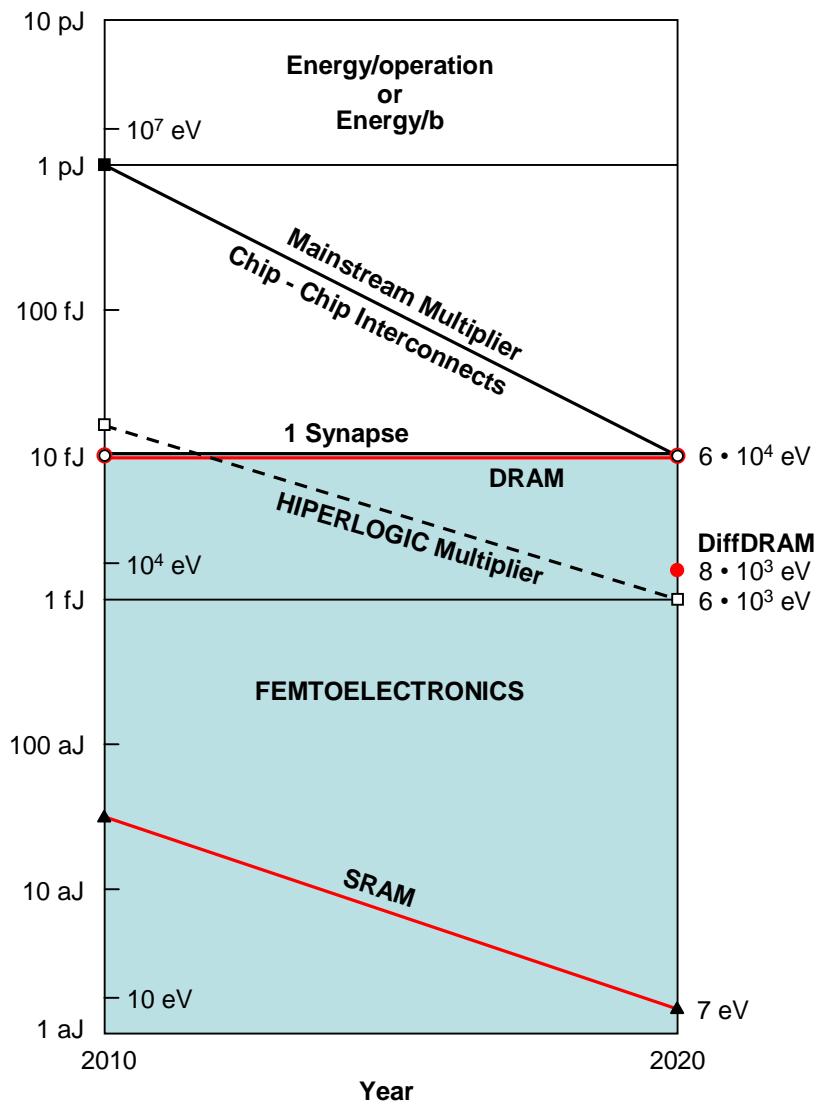
130k wafers per month 12" fab, 150,000 kW

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Estimated Electrical Power (kW) for Lithography in a 32nm 150 MW Gigafactory

## • A New Sustainable Roadmap: Energy

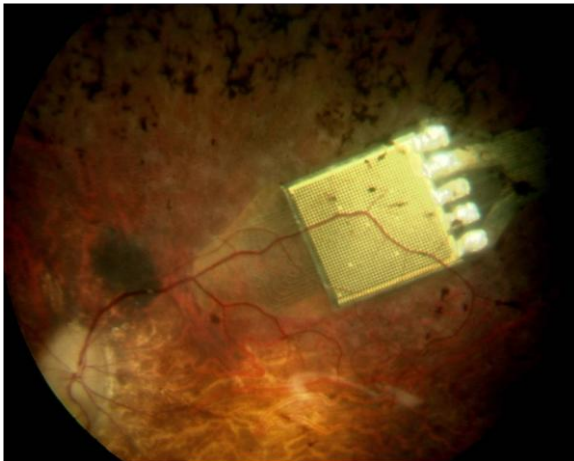
- **Analog-Digital Interfaces (chapter 4)** by Matthias Keller and Yiannos Manoli, Chair for Microelectronics, University Freiburg, Germany, and Boris Murmann, Stanford University, USA
- **Interconnects and Transceivers (chapter 5)** by Bernd Hoefflinger.
- **Power-Efficient Design Challenges (chapter 9)** by Barry Pangrle, Low-Power Solutions Architect, Mentor Graphics, Fremont, CA, USA.
- **Superprocessors and Supercomputers (chapter 10)** by Peter Roth, Manager Hardware Development, IBM R&D Laboratory Germany, and Colleagues.
- **Towards Terabit Memory (chapter 11)** by Bernd Hoefflinger.
- **Energy Harvesting and Chip Autonomy (chapter 19)** by Yiannos Manoli, Chair for Microelectronics, University Freiburg, and Institute for Micro and Information Technology, Villingen-Schwenningen, Germany, and his Teams.
- **The Energy Crisis (chapter 20)** by Bernd Hoefflinger.



Energy per Bit for chip-chip interconnects and various memories. Energy per multiplication for multipliers. Switching energy of a synapse in the human brain.

## 3D-Integrated Systems-on-Chip and Silicon Brains

- **Requirements and Markets (chapter 6)** by Bernd Hoefflinger.
- **3D Integration for Wireless Mobile Multimedia (chapter 12)** by Georg Kimmich, Product Manager, ST-Ericsson, Grenoble, France.
- **The Next Generation Mobile User-Experience (chapter 13)** by Greg Delagi, Senior Vice President, Texas Instruments, Dallas, TX, USA.
- **MEMS (Micro-Electro-Mechanical Systems) for Automotive and Consumer Applications (chapter 14)** by Jiri Marek, Senior Vice President, and Udo Gomez, Director of Engineering, Robert Bosch GmbH, Reutlingen, Germany.
- **Vision Sensors and Cameras (chapter 15)** by Bernd Hoefflinger.
- **Digital Neural Networks for New Media (chapter 16)** by Lambert Spaanenburg and Suleiman Malki, Lund Technical University, Sweden.
- **Retinal Implants for Blind Patients (chapter 17)** by Albrecht Rothermel, Chair for Microelectronics, University Ulm, Germany.
- **Silicon Brains (chapter 18)** by Bernd Hoefflinger.
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Subretinal Implant with 1800 active photoreceptors/stimulators

## Requirements-Driven R&D and Product Generation

- **From Microelectronics to Nanoelectronics (chapter 2)** by Bernd Hoefflinger.
- **The Extreme-Technology Industry (chapter 21)** by Bernd Hoefflinger.
- **Education and Research for the Age of Nanoelectronics (chapter 22)** by Bernd Hoefflinger.
- **2020 World with Chips (chapter 23)** by Bernd Hoefflinger.

Bernd Hoefflinger served as Director of the Institute for Microelectronics Stuttgart, Germany, a certified, contract research and manufacturing institute. He started his career as an assistant professor at Cornell University. Returning to Germany, he became the first MOS Product manager at Siemens. As a co-founder of the University of Dortmund, Germany, he built one of the first university pilot lines for IC's in Europe. Again in the USA, he served as Head of Electrical Engineering at the University of Minnesota and at Purdue University, before taking on the build-up in Stuttgart.

Chips 2020

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